UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/556,398	11/10/2005	Francois Droz	90500-000067/US	6278

30593 7590 02/14/2008
HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
MAI, THIEN T	

ART UNIT	PAPER NUMBER
2887	

MAIL DATE	DELIVERY MODE
02/14/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/556,398	DROZ, FRANCOIS	
	Examiner	Art Unit	
	Thien T. Mai	2887	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. Acknowledgement is hereby made of the preliminary amendment filed 11/10/2005

Objections

2. Applicant is respectfully requested to insert the priority claiming in the first paragraph of the specification

3. Claim 1 line 3, replace "a generally flat insulating support called a substrate" with --a flat insulating substrate--

4. Claim 6, it is indefinite as to which tool is considered "adequate" and how much is considered "adequate"

5. Claim 7 line 2, remove "sensibly"

6. Claims 3 and 7: it is unclear what is referred to by "its"

7. Claim 8 "the substrate" lacks antecedent basis. There are multiple types of substrate being claimed. Please clarify which.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim(s) 1-14 is/are rejected under 35 U.S.C. 102(b) as being anticipated by Fidalgo (5,598,032)

Fidalgo discloses:

1. Assembly process characterized by the following steps:

placing the substrate on a work surface, the face including conductive tracks (5, 15) being oriented upwards,

placing the electronic component (7) into a cavity (17) of the substrate situated in a zone including the conductive tracks, the conductive areas of the component coming into contact with the corresponding tracks of the substrate (FIG. 5),

applying a layer of insulating material (i.e. adhesived substrate 4) which extends at the same time on the component (7) and at least on a substrate zone surrounding said component, in such a way that the electric connection between the conductive areas and conductive tracks is ensured by the pressure of the insulating layer on the component (the connection is held by the adhesion pressure holding the component chip with the surrounding substrates; or the pressure of the insulating layer 4 on the component due to tightness causing the chip to be held within the cavity).

2. Process according to claim 1 wherein the electronic component is made up of a chip provided with contacts on one of its faces, said contacts being set off on a conductive film constituting the contact areas that extend the contacts of the chip, the opposite face of the chip being coated by an insulating material (i.e. adhesive).

3. Process according to claim 1 wherein the layer of insulating material is made up of a first substrate (4) including a cavity into which the component is inserted by its

coated face, the contact areas of said component connecting with corresponding conductive areas of a second substrate (3) placed on the work surface (fig 5).

4. Process according to claim 1 wherein the electronic component is made up of a chip provided with contacts on one of its faces, said contacts being set off on a conductive film constituting the contact areas that extend the contacts of the chip (fig. 5)

5. Process according to claim 1 wherein the electronic component is made up of a chip provided with contacts on one of its faces, said contacts being set off on a conductive film constituting the contact areas that extend the contacts of the chip (fig. 5), the layer of insulating material is made up of a first substrate including a cavity in which the chip of the component is inserted, the contact areas of said component being applied against the surface of the substrate connecting with corresponding conductive areas of a second substrate placed on the work surface (fig. 5).

6. Process according to claim 5 wherein the cavity of the component is obtained by heating the chip (inherently by soldering to provide contacts) of the component then pushing said chip into the substrate material by means of adequate tooling, the contact areas of said component being applied against the surface of the substrate.

7. Process according to claim 1 wherein the electronic component is made up of a chip provided with sensibly flat contacts on one of its faces.

8. Process according to claim 7 wherein the layer of insulating material is made up of a first substrate including a cavity into which the chip is inserted, the contacts of said chip showing on the surface level of the substrate are connected with corresponding conductive areas of a second substrate placed on the work surface.

9. Process according to claim 1 wherein the cavity of the component is inherently known in the art to be made up by milling or by stamping a window.

10. Process according to claim 8 wherein the cavity of the chip is obtained by heating (inherently by soldering) then pressing said chip into the material of the substrate by means of adequate tooling, the contact areas of said chip showing on the surface level of the substrate.

11. Process according to claim 1 wherein the electronic component is made up of a module including a set of flat contacts on one of its faces and on the opposite face conductive areas linked to each contact of the set.

12. Process according to claim 1 wherein the module is inserted into a cavity provided with a window cut into a first substrate with a thickness approximately equal to that of the module, the set of flat contacts shows on the surface level of said substrate and the conductive areas of the opposite face lean against the conductive tracks of a second substrate assembled on the first substrate (Fig. 1+)

13. Process according to claim 12, wherein at least one module or a supplementary chip is mounted in one of the substrates, said module including conductive areas connected by pressure on the corresponding conductive tracks of either of the substrates.

14. Process according to claim 13 wherein it includes a supplementary step of gluing and pressing the assembly formed by the superposition of the substrates.

Remarks

Applicant indicated 11/10/2005 that claims 1-14 were presented in the preliminary amendment; however, it appears only claims 1-4 were amended and submitted as of 01/31/2008. The Examiner realizes that the Publication 20060226237 of the current application has 14 claims. Therefore, this office action is based on claims 1-14 in the Publication.

The Examiner notes that a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). In other words, the preamble is not given patentable weight unless incorporated in the claim body.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Houdeau et al. (6072698), German publication (DE 4401458 A1)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien T. Mai whose telephone number is 571-272-8283. The examiner can normally be reached on Monday through Friday, 8:00 - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve S. Paik can be reached on 571-272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thien T Mai/
Examiner, Art Unit 2887

/Seung H Lee/
Primary Examiner,
Art Unit 2887